Microelectronics ECSE 335

Laboratory No. 5

Design, Simulation and Validation of an Interface (Buffer) Circuit Between a Differential Amplifier and Class AB Output Stage

Purpose:

Design a BJT circuit that maximizes the gain of a multistage cascade consisting of a front-end differential amplifier and a class-AB output amplifier, and further establish the correct DC biasing of the two stages so that the maximum output signal swing is made possible.

Equipment Required:

a. Computer
b. SPICE Simulator (student choice)
c. Test Bench: DC Voltage supplies, Function Generator and Oscilloscope
d. Components:
    i. Student decision but must be available from the parts-master on the 4th floor service counter in the Trottier building.
    ii. It is suggested to assemble some of the circuit components prior to entering the laboratory to save time.

Write-Up Requirements:

A good laboratory report should contain a **brief** description of what the experiment was about, including circuit diagrams, and what you did, your data, your results, and anything else called for in the assignment, such as questions inserted in the laboratory description. Answers to these questions require observations that need to be made at the time you do the experiment.

While not always explicitly spelled out in any one laboratory, the use of SPICE should be used by

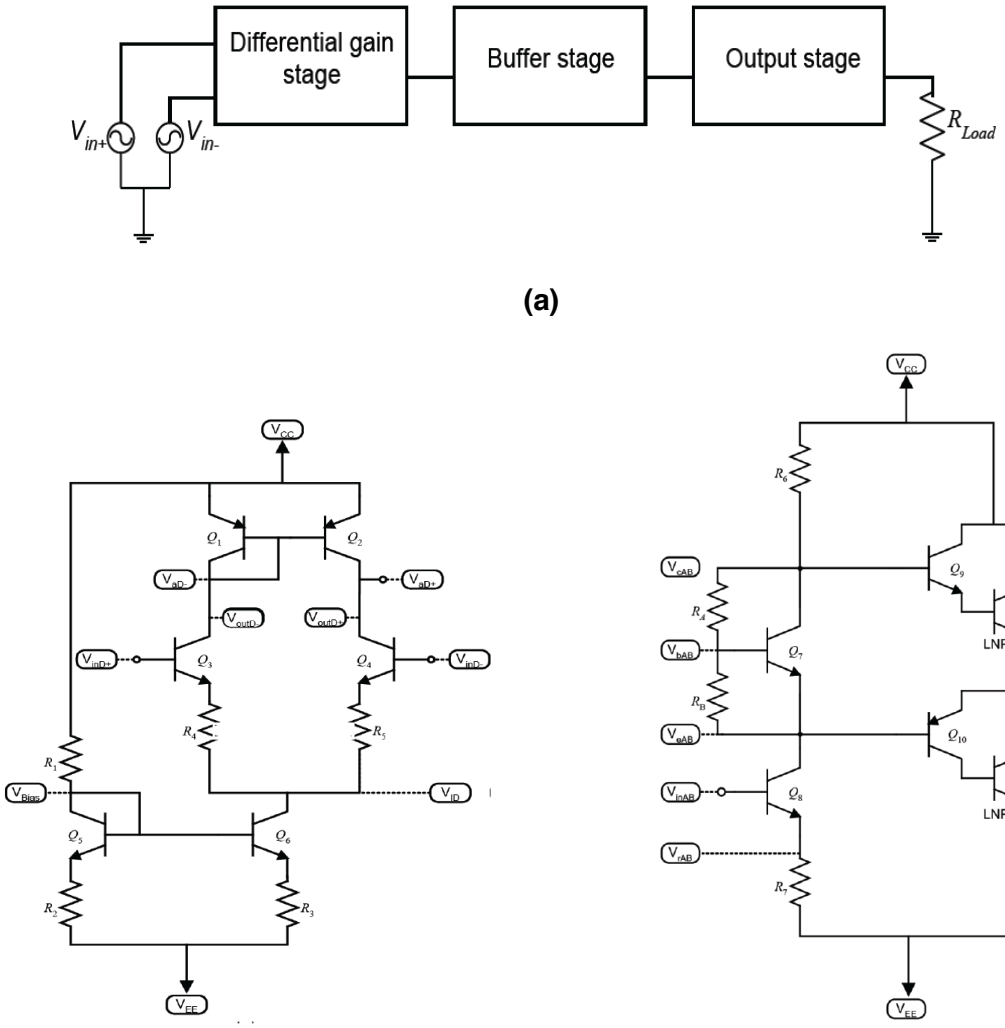

Figure 5.1: Multistage amplifier cascade: (a) block diagram, (b) differential gain stage, and (c) class AB output stage.

the student to predict the experimental outcomes. SPICE results should be compared to that obtained by measurement, and any differences explained or justified.

The laboratory report should be written using the IEEE paper style consisting of a **double-column single-space format**, and must adhere to the following when necessary:

1. Title page - Title of the assignment/project, authors' name, and course name.
2. Abstract - Abstract of the assignment/project report.
3. Introduction
4. Main body of the assignment/project report including figures.
6. Conclusions
7. References
8. Appendices

Buffer Stage

A multi-stage amplifier is to be constructed using a cascade of a differential gain stage combined with an output stage capable of driving large loads (i.e., low resistance loads). However, arbitrary connection of two independent amplifier stages will be subject to loading and changing DC biasing effects; essentially reducing their effectiveness. One method that is used to allow the interconnection of two independent stages is to add an interface circuit between the two stages that provides a high input impedance to the first stage and a low output impedance to drive the second stage. Such a circuit would easily be fulfilled with a voltage follower or buffer circuit. In addition, the designer must also ensure that the bias conditions are not significantly altered by the interface circuit. The latter is particularly important, as the DC level of the gain stage's output and the output stage's input must be kept the same as when they were tested individually. In this experiment, you must design a transistor-based circuit which will accomplish this function. Notice that, thanks to this circuit, the output stage will not require the input biasing circuit of Figure 4.3 of Lab. 4.

Preparation

The student should make use of hand analysis and/or a circuit simulation tool such as SPICE to answer the following questions.

1. Determine the design specifications of the circuit which you believe are required for proper operation of the multistage amplifier. Be sure to have a logical reasoning as to why each specification you decide upon is required. Some common design specifications are: Bandwidth, gain, input resistance, output resistance, input DC insensitivity, input maximal swing, and output maximal swing.
2. Based on the design specifications you have decided upon, create a circuit capable of meeting these specs and, if necessary, modify the specifications slightly if you deem them ultimately unattainable. Determine the component values and explain the functioning of your interface circuit. Provide a schematic of the design.
3. Determine the input and output resistances of the circuit.
4. Plot the time domain output of the circuit to an input which is comparable to the maximum expected differential amplifier output.
5. Plot the frequency response of the circuit. Ensure that the parasitic capacitors are accounted for.
6. Plot the voltage transfer curve of the circuit. Document the maximal output and input ranges.

7. Comment on the advantages and disadvantages of your design.

Experiment

For this laboratory, you can use a biasing network similar to that in Figure 4.3 of Lab. 4 to test the circuit as a standalone. Perform the following in tests in succession (make sure to use a 10X probe when required!):

1. Measure all DC voltages and infer the DC currents where possible. As for all results in this experiment, compare with expected (simulations and calculations) values.
2. Plot the time domain output of the circuit to an input which is comparable to the maximum expected differential amplifier output.
3. Plot the voltage transfer characteristic of the circuit. Document the maximal output and input ranges.
4. Plot the frequency response and find the 3-dB points. Use the 10X probe.
5. Measure the output and input resistances of your circuit.

This concludes this lab.