Department Of Electrical & Computer Engineering
Course ECSE 335 **Session 24/Fall**

Introduction To Microelectronic Circuits
Assignment #4

Differential Amplifier Biasing and Amplification

Choose any 3 of the following 5 amplifier design problems:

1. Bias a NMOS differential amplifier with V/I load in a 1 um CMOS process described by $\mu_n C_{OX}$ = 0.1 mA/V, V_t =0.5 V and λ'_n=2x10^{-7} m/V such that it has a DC gain whose magnitude is at least 40 V/V and an output DC bias point of 2.2 V. Assume a 3.3 V supply level and an input common-mode level of 1.65 V. Ensure that each device is operating in its saturation region. Verify your result using SPICE.

2. Bias a PMOS differential amplifier with V/I load in a 1 um CMOS process described by $\mu_n C_{OX}$ = 0.05 mA/V, V_t =-0.6 V and λ'_n=2x10^{-7} m/V such that it has a DC gain whose magnitude is equal to 10 V/V and an output DC bias point of 1.0 V. Assume a 5.0 V supply level and an input common-mode level of 1.65 V. Ensure that each device is operating in its saturation region. Verify your result using SPICE.

3. Bias a NMOS differential amplifier with V/V load in a 1 um CMOS process described by $\mu_n C_{OX}$ = 0.1 mA/V, Vt =0.5 V and λ'_n=2x10^{-7} m/V such that its two output are set at 1.65 V. Assume a 3.3 V supply level with V_{G1}=V_{G2}=V_{CM}= 1.65 V. Select the biasing conditions so that the magnitude of the small-signal current-to-differential-voltage ratio $i_{d,2}/v_d$ is 50 μA/V. Ensure that each device is operating in its saturation region. Verify your result using SPICE.

4. Bias a PMOS differential amplifier with V/V load in a 1 um CMOS process described by $\mu_n C_{OX}$ = 0.05 mA/V, V_t =-0.6 V and λ'_n=2x10^{-7} m/V such that its two output are set at 1.0 V. Assume a 3.3 V supply level with V_{G1}=V_{G2}=V_{CM}= 1.65 V. Select the biasing conditions so that the magnitude of the small-signal

current-to-differential-voltage ratio $i_{d,2}/v_d$ is 100 μA/V. Ensure that each device is operating in its saturation region. Verify your result using SPICE.

5. Design an npn differential amplifier with V/I load in a bipolar process described by $V_{A,n} = V_{A,p} = 100$ V and $I_S = 1 \times 10^{-15}$ A. Set the output Q-point at 6 V, while using a DC power supply of 10 V and an input common-model level of 5 V. Set the magnitude of the small-signal voltage gain to 30 V. Ensure that the devices are operating in their active region. Verify your result using SPICE. Assume that the current source biasing is derived from a single pnp transistor with finite output resistance, i.e., a current source in parallel with an AC coupled resistor.