Department Of Electrical & Computer Engineering
Course ECSE 335 **Session 24/Fall**

Introduction To Microelectronic Circuits
Assignment #3

Differential Amplifier Biasing:

Choose any three of the following 6 biasing problems:

1. Bias a NMOS differential amplifier with V/I load in a 1 um CMOS process described by $\mu_n C_{OX}$ = 0.1 mA/V, V_t =0.5 V and λ'_n=2x10^{-7} m/V such that its output is set at 2.2 V. Assume a 3.3 V supply level and an input common-mode level of 1.65 V. Ensure that each device is operating in its saturation region. Verify your result using SPICE.

2. Bias a NMOS differential amplifier with V/I load in a 1 um CMOS process described by $\mu_n C_{OX}$ = 0.1 mA/V, V_t =0.5 V and λ'_n=2x10^{-7} m/V such that its output is set at 2.2 V. Assume a 3.3 V supply level with V_{G1}= 1.65 V and V_{G2}=2.0 V. Ensure that each device is operating in its saturation region. Verify your result using SPICE.

3. Bias a NMOS differential amplifier with V/I load in a 1 um CMOS process described by $\mu_n C_{OX}$ = 0.1 mA/V, Vt =0.5 V and λ'_n=2x10^{-7} m/V such that its output is set at 1.65 V. Assume a 3.3 V supply level with V_{G1}=V_{G2}= 1.65 V and $V_{D,1}$=2.2 V. Ensure that each device is operating in its saturation region. Verify your result using SPICE.

4. Bias a PMOS differential amplifier with V/I load in a 1 um CMOS process described by $\mu_n C_{OX}$ = 0.05 mA/V, V_t =-0.6 V and λ'_n=2x10^{-7} m/V such that its output is set at 1.0 V. Assume a 5.0 V supply level and an input common-mode level of 1.65 V. Ensure that each device is operating in its saturation region. Verify your result using SPICE.

5. Bias a NMOS differential amplifier with V/V load in a 1 um CMOS process described by $\mu_n C_{OX}$ = 0.1 mA/V, Vt =0.5 V and $\lambda'_n=2x10^{-7}$ m/V such that its two output are set at 1.65 V. Assume a 3.3 V supply level with $V_{G1}=V_{G2}=V_{CM}$= 1.65 V. Ensure that each device is operating in its saturation region. Verify your result using SPICE.

6. Bias a PMOS differential amplifier with V/V load in a 1 um CMOS process described by $\mu_n C_{OX}$ = 0.05 mA/V, V_t =-0.6 V and $\lambda'_n=2x10^{-7}$ m/V such that its two output are set at 1.0 V. Assume a 3.3 V supply level with $V_{G1}=V_{G2}=V_{CM}$= 1.65 V. Ensure that each device is operating in its saturation region. Verify your result using SPICE.