Department Of Electrical & Computer Engineering

Course ECSE 335 **Session 24/Fall**

Introduction To Microelectronic Circuits
Assignment 2

Amplifier Gain:

Choose any three of the following 5 amplifier design problems:

1. Design an CS NMOS amplifier in a 1 µm CMOS process described by $\mu_n C_{OX}$ = 0.1 mA/V, V_t =0.5 V and $\lambda'_n=2x10^{-7}$ m/V such that it has a DC gain whose magnitude is at least 40 V/V and a DC bias point of 1.65 V using a 3.3 V supply. Set the source terminal to 0 V. Assume the current source is ideal. Verify your result using SPICE.

2. Design a CG NMOS amplifier in a 1 µm CMOS process described by $\mu_n C_{OX}$ = 0.1 mA/V, V_t =0.5 V and $\lambda'_n=2x10^{-7}$ m/V such that its output is set at 2.2 V and it has a DC magnitude gain of at least 30 V/V. Assume a 3.3 V supply level and that the source terminal is set at 1.2 V. Ensure that the device is operating in its saturation region. Assume the current source is ideal. Verify your result using SPICE.

3. Design a CE npn amplifier with an emitter degenerate resistor in a bipolar process described by $V_{A,n} = V_{A,p}$ = 100 V and $I_S =1x10^{-15}$ A such that its output is set at 8 V. Assume a 10 V supply level and that one side of the degenerate resistor is set to 0 V. Design for a DC gain whose magnitude is equal to 90 V/V. Ensure that the device is operating in its active region. Assume that the current source biasing is derived from a single pnp transistor with finite output resistance. A current source with an AC coupled resistor in parallel will suffice as a circuit model for the current source, i.e.

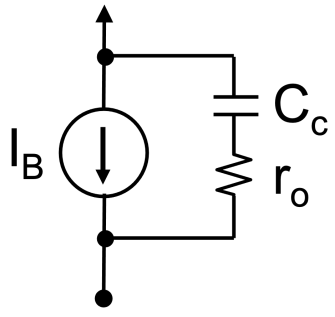

Fig. 1

4. Design a CE npn amplifier with resistor degeneration in a bipolar process described by $V_{A,n} = V_{A,p} = 100$ V and $I_S = 1 \times 10^{-15}$ A such that its output is set at 5 V and has a DC gain with a magnitude of exactly 20 V/V. Assume a ±12 V split supply level and that the base terminal is set at 0 V. Ensure that the device is operating in its active region. Also assume that the current source biasing is derived from a single pnp transistor with finite output resistance (see Fig. 1). Verify your result using SPICE.

5. Design a CD PMOS amplifier in a 1 µm CMOS process described by $\mu_p C_{OX} = 0.05$ mA/V, $V_t = -0.6$ V and $\lambda'_p = 2 \times 10^{-7}$ m/V such that its output is set at 1.65 V and has a DC gain of at least 0.85 V/V. Assume a 3.3 V supply level. Ensure that the device is operating in its saturation region. Assume the current source is ideal. Verify your result using SPICE.